## CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letter Patent is:

1. A method of forming a dual workfunction high performance MOSFET/EDRAM array having a gate conductor guard ring formed around the array region, said method comprising the steps of:

(a) providing a memory structure having at least one array region and at least one support region, wherein said at least one array region and said at least one support region are separated by an isolation region, wherein said at least one array region includes a plurality of dynamic random access memory (DRAM) cells embedded in a substrate, wherein adjacent DRAM cells are connected to each other through bitline diffusion regions which are capped with an oxide capping layer;

(b) forming a patterned nitride layer on all exposed surfaces in said at least one array region and on a portion of said isolation region;

(c) forming a gate oxide on said substrate in said at least one support region;

(d) forming a stack comprising a first polysilicon layer and a dielectric capping layer on all exposed surfaces of said memory structure;

(e) removing said dielectric capping layer, said first polysilicon layer and said nitride layer from said at least one array region;

(f) forming wordlines over said plurality of DRAM cells in said at least one array region;

(g) forming spacers on exposed sidewalls of said wordlines in said at least one array region as well as on exposed sidewalls of said stack remaining in said structure;

(h) forming a block mask over the at least one support region and at least a portion of one of said DRAM cells that is adjacent to said isolation region, whereby said block mask does not cover said oxide capping layer;

(i) removing said oxide capping layer over said bitline diffusion regions and stripping said block mask;

(j) forming a patterned second polysilicon layer over the at least one array region and said stack which is present on said isolation region, and removing said dielectric capping layer in said at least one support region;

(k) forming a doped glass material layer over all surfaces in said at least one array region and said at least one support region;

(l) patterning said doped glass material layer so as to form hard masks in said at least one array region and said at least one support region, whereby said hard mask in said at least one array region defines a bitline of the memory structure and said hard mask in said at least one support region defines a support gate region;

(m) removing exposed second polysilicon layer from said at least one array region and said isolation region, while simultaneously removing exposed portions of said first polysilicon layer in said at least one support region, whereby a gate conductor guard ring is formed on said isolation region and said support gate region is formed in said at least one support region;

(n) removing said hard masks from said at least one array region and from said at least one support region and forming a screen oxide layer on any exposed silicon surfaces;

(o) forming source and drain regions about said support gate region; and

(p) removing oxide overlying said bitline, support gate region, and source and drain regions so as to expose silicon surfaces and saliciding the exposed silicon surfaces so as to provide salicide regions over said bitline, said gate region and said source and drain regions.

2. The method of Claim 1 wherein said isolation region is a shallow trench isolation region.

3. The method of Claim 1 wherein each of said DRAM cells includes at least a gate conductor region formed in a top portion of a deep trench, and a trench polysilicon formed in a lower portion of said deep trench, said gate conductor and said trench polysilicon being separated by a trench oxide.

4. The method of Claim 3 wherein each of said DRAM cells includes a collar oxide region and a buried strap outdiffusion region.

5. The method Claim 1 wherein said patterned nitride layer is formed by deposition, lithography and etching.

6. The method of Claim 1 wherein said gate oxide is thermally grown.

7. The method of Claim 1 wherein said gate oxide has a thickness of from about 1 to about 15 nm.

8. The method of Claim 1 wherein said stack is formed from a deposition process selected from the group consisting of chemical vapor deposition (CVD), plasma-assisted CVD, sputtering, spin-on coating and chemical solution deposition.

9. The method of Claim 1 wherein step (e) includes applying a mask to cover the at least one support region and etching through said dielectric capping layer, said first polysilicon layer and said nitride layer.

10. The method of Claim 9 wherein said etching is conducted by two separate etching steps.

11. The method of Claim 1 wherein said wordlines comprise a conductive metal and a top insulating layer.

12. The method of Claim 11 wherein said conductive metal is W/WN and said top insulator is SiN.

13. The method of Claim 1 wherein said wordlines are formed by deposition, lithography and etching.

14. The method of Claim 1 wherein said spacers of step (g) are formed by deposition and lithography.

15. The method of Claim 1 wherein step (i) includes an etching step.

16. The method of Claim 1 wherein said doped glass material is replaced with a bilayer resist.

17. The method of Claim 1 wherein step (l) includes lithography and an anisotropic etching process.

18. The method of Claim 1 wherein step (m) includes a selective etching process.

19. The method of Claim 1 further comprising forming an interlevel dielectric on said structure and providing via openings in said interlevel dielectric exposing said source and drain regions.

20. A method of forming a dual workfunction high performance MOSFET/EDRAM array comprising the steps of:

(a) providing a memory structure having at least one array region and at least one support region, wherein said at least one array region and said at least one support region are separated by an isolation region, wherein said at least one array region includes a plurality of dynamic random access memory (DRAM) cells embedded in a substrate, wherein adjacent DRAM cells are connected to each other through bitline diffusion regions which are capped with an oxide capping layer;

(b) forming a patterned nitride layer on all exposed surfaces in said at least one array region and on a portion of said isolation region;

(c) forming a gate oxide on said substrate in said at least one support region;

(d) forming a stack comprising a first polysilicon layer and a dielectric capping layer on all exposed surfaces of said memory structure;

(e) removing said dielectric capping layer, said first polysilicon layer and said nitride layer from said at least one array region;

(f) forming wordlines over said plurality of DRAM cells in said at least one array region;

(g) forming spacers on exposed sidewalls of said wordlines in said at least one array region as well as on exposed sidewalls of said stack remaining in said structure;

(h) anisotropically etching said memory structure so as to remove said oxide capping layer thereby exposing said bitline diffusion regions in said at least one array region, while simultaneously removing said dielectric capping layer over said isolation region and in said at least one support region;

(i) depositing an undoped layer of polysilicon over all exposed surfaces of said memory structure;

(j) patterning said undoped layer of polysilicon so as to simultaneously form a bitline in said at least one array region and a gate region in said at least one support region;

(k) forming a screen oxide layer on any exposed silicon surfaces;

(l) forming sidewall spacers about said gate region;

(m) forming source and drain regions about said gate region; and

(n) removing oxide overlying said bitline, gate region, and source and drain regions so as to expose silicon surfaces and saliciding said exposed silicon surfaces so as to provide salicide regions over said bitline, said gate region and said source and drain regions.

21. The method of Claim 20 wherein said isolation region is a shallow trench isolation region which extends into one of said DRAM cells.

22. The method of Claim 20 wherein each of said DRAM cells includes at least a gate conductor region formed in a top portion of a deep trench, and a trench polysilicon formed in a lower portion of said deep trench, said gate conductor and said trench polysilicon being separated by a trench oxide.

23. The method of Claim 22 wherein each of said DRAM cells includes a collar oxide region and a buried strap outdiffusion region.

24. The method Claim 20 wherein said patterned nitride layer is formed by deposition, lithography and etching.

25. The method of Claim 20 wherein said gate oxide is thermally grown.

26. The method of Claim 20 wherein said gate oxide has a thickness of from about 1 to about 15 nm.

27. The method of Claim 20 wherein said stack is formed from a deposition process selected from the group consisting of chemical vapor deposition (CVD), plasma-assisted CVD, sputtering, spin-on coating and chemical solution deposition.

28. The method of Claim 20 wherein step (e) includes applying a mask to cover the at least one support region and etching through said dielectric capping layer, said first polysilicon layer and said nitride layer.

29. The method of Claim 28 wherein said etching is conducted by two separate etching steps.

30. The method of Claim 20 wherein said wordlines comprise a conductive metal and a top insulating layer.

31. The method of Claim 30 wherein said conductive metal is W/WN and said top insulator is SiN.

32. The method of Claim 20 wherein said wordlines are formed by deposition, lithography and etching.

33. The method of Claim 20 wherein said spacers of step (g) are formed by deposition and lithography.

34. The method of Claim 1 wherein step (j) includes lithography and etching.

35. The method of Claim 20 further comprising forming an interlevel dielectric on said structure and providing via openings in said interlevel dielectric exposing said source/drain regions.

36. A method of forming a dual workfunction high performance MOSFET/EDRAM array having a local interconnect composed of the same material as that of the wordline of the memory structure, said method comprising the steps of:

(a) providing a memory structure having at least one array region and at least one support region, wherein said at least one array region and said at least one support region are separated by an isolation region, wherein said at least one array region includes a plurality of dynamic random access memory (DRAM) cells embedded in a substrate, wherein adjacent DRAM cells are connected to each other through bitline diffusion regions which are capped with an oxide capping layer;

(b) forming a patterned nitride layer on all exposed surfaces in said at least one array region and on a portion of said isolation region;

(c) forming a gate oxide on said substrate in said at least one support region;

(d) forming a stack comprising a first polysilicon layer and a dielectric capping layer on all exposed surfaces of said memory structure;

(e) removing said dielectric capping layer, said first polysilicon layer and said nitride layer from said at least one array region and a portion of said at least one support region;

(f) doping a portion of said substrate in said support region so as to form a diffusion region for subsequent formation of a local interconnect contact thereon;

(g) forming wordlines over said plurality of DRAM cells in said at least one array region, while simultaneously forming a local interconnect in said at least one support region above said diffusion region, wherein said wordlines and said local interconnect are composed of the same material;

(h) forming spacers on exposed sidewalls of said wordlines in said at least one array region, and said local interconnect and remaining stack in said at least one support region, said remaining stack defining a support gate region of said structure;

(i) removing any exposed oxide over said bitline diffusion regions;

(j) forming a patterned second polysilicon layer over the at least said at least one array region and said stack which is overlaying said isolation region, and removing said dielectric capping layer in said at least one support region;

(k) forming a doped glass material layer over all surfaces in said at least one array region and said at least one support region;

(l) patterning said doped glass material layer so as to form a hard mask in said at least one array region, whereby said hard mask in said at least one array region defines a bitline of the memory structure;

(m) removing said hard mask from said at least one array region and forming an oxide layer on all exposed silicon surfaces;

(n) forming source and drain regions about said gate region; and

(p) removing oxide overlying said bitline, support gate region, and source and drain regions so as to expose said silicon surfaces and saliciding said silicon surfaces so as to provide salicide regions over said bitline, said support gate region and said source and drain regions.

37. The method of Claim 36 wherein said isolation region is a shallow trench isolation region.

38. The method of Claim 36 wherein each of said DRAM cells includes at least a gate conductor region formed in a top portion of a deep trench, and a trench polysilicon formed in a lower portion of said deep trench, said gate conductor and said trench polysilicon being separated by a trench oxide.

39. The method of Claim 38 wherein each of said DRAM cell includes a collar oxide region and a buried strap outdiffusion region.

40. The method Claim 36 wherein said patterned nitride layer is formed by deposition, lithography and etching.

41. The method of Claim 36 wherein said gate oxide is thermally grown.

42. The method of Claim 36 wherein said gate oxide has a thickness of from about 1 to about 15 nm.

43. The method of Claim 36 wherein said stack is formed from a deposition process selected from the group consisting of chemical vapor deposition (CVD), plasma-assisted CVD, sputtering, spin-on coating and chemical solution deposition.

44. The method of Claim 36 wherein step (e) includes applying a mask to cover the at least one support region and etching through said dielectric capping layer, said first polysilicon layer and said nitride layer.

45. The method of Claim 44 wherein said etching is conducted by two separate etching steps.

46. The method of Claim 36 wherein said wordlines and said local interconnect are both comprised of a conductive metal and a top insulating layer.

47. The method of Claim 46 wherein said conductive metal is W/WN and said top insulator is SiN.

48. The method of Claim 36 wherein said wordlines and said local interconnect are formed simultaneously by deposition, lithography and etching.

49. The method of Claim 36 wherein said spacers of step (h) are formed by deposition and lithography.

50. The method of Claim 36 wherein step (j) includes an etching step.

51. The method of Claim 36 wherein said doped glass material is replaced with a bilayer resist.

52. The method of Claim 36 further comprising forming an interlevel dielectric on said structure and providing via openings in said interlevel dielectric exposing said source and drain regions.

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53. A dual workfunction high-performance support MOSFET/EDRAM array comprising at least one support region and at least one array region, said array region and said support region being separated by an isolation region, and at least a gate conductor guard ring formed around said array region on top of said isolation region, wherein said gate conductor guard ring prevents trapping of a stringer of polysilicon on said isolation region.

54. The dual workfunction high-performance support MOSFET/EDRAM array of Claim 53 wherein said array region includes a plurality of DRAM cells embedded in a semiconductor substrate.

55. The dual workfunction high-performance support MOSFET/EDRAM array of Claim 54 wherein wordlines overlay each of said DRAM cells and a bitline overlays said wordlines.

56. The dual workfunction high-performance support MOSFET/EDRAM array of Claim 54 wherein each of said DRAM cells are vertical DRAMs.

57. A dual workfunction high-performance support MOSFET/EDRAM array comprising at least one support region having a local interconnect formed therein and at least one array region having at least one wordline formed therein, said at least one array region and said at least one support region are separated by an isolation region, and said at least one wordline and said local interconnect are comprised of identical material.

58. The dual workfunction high-performance support MOSFET/EDRAM array of Claim 57 wherein said at least one array region includes a plurality of DRAM cells embedded in a semiconductor substrate.

59. The dual workfunction high-performance support MOSFET/EDRAM array of Claim 58 wherein said DRAM cells are vertical DRAMs.